SOLUTION

Subject Code : REE 602 **Subject : MICROPROCESSOR**

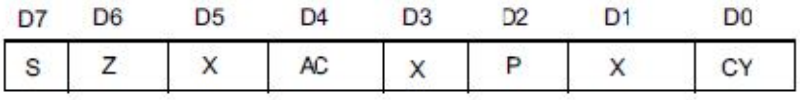
B.Tech.: Semester: VI

FIRST SESSIONAL EXAMINATION, EVEN SEMESTER, (2019-2020)

Branch : Electrical Engineering / Electrical & Electronics Engineering

SECTION – A

1. Attempt all questions in brief. **(1*5 = 5)**

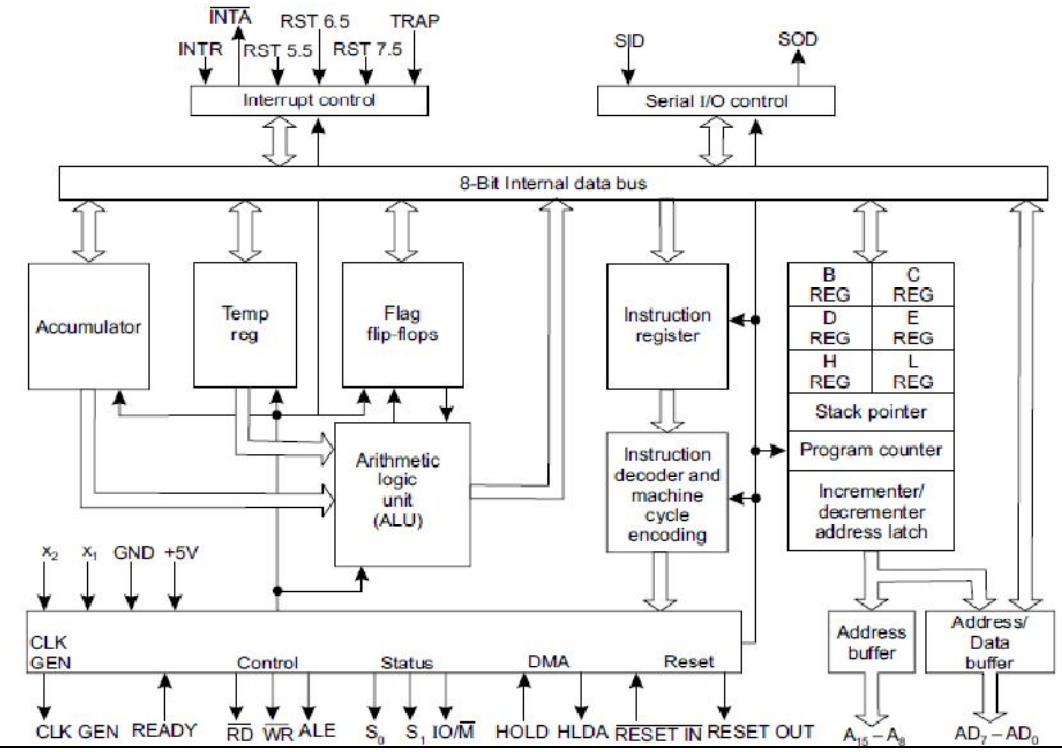
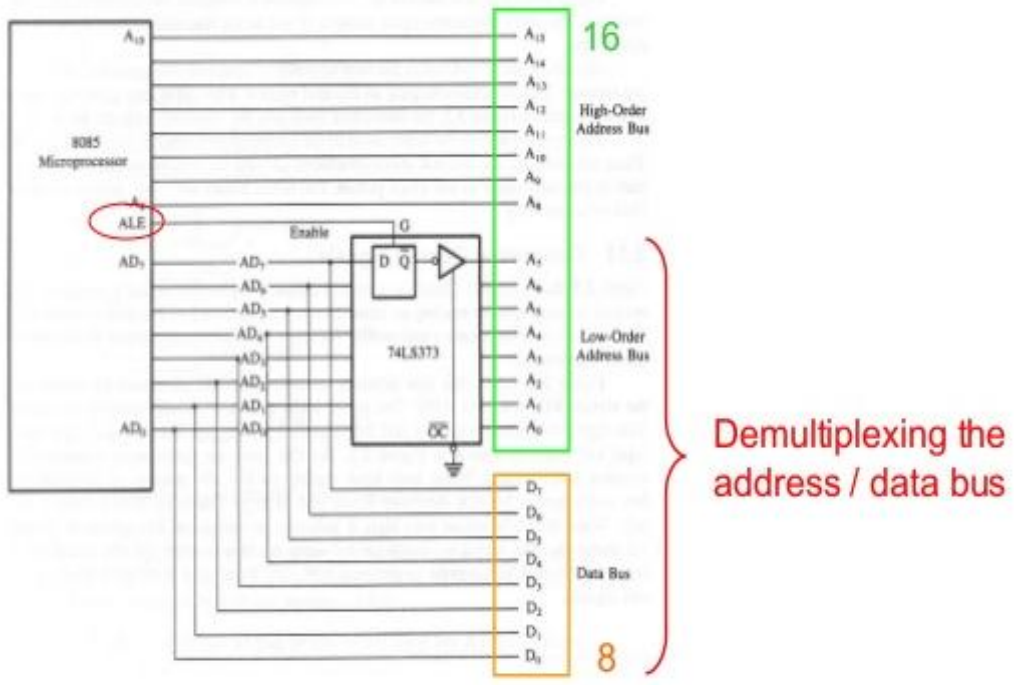
Q N	QUESTION	Marks	CO	BL
a.	Write basic operations of microprocessor. Answer : 1. Memory Read : Reads data (or instruction) from Memory 2. Memory Write : Write data (or instruction) into Memory 3. I/O Read : Accepts data from input devices. 4. I/O Write : Sends data to output devices.	1	1	1
b.	What are interfacing logical devices? Answer : Gates, Buffer, Decoders, multiplexer and Latches etc.	1	1	1
c.	Why data bus is bi-directional? Answer : The microprocessor has to fetch (read) the data from memory or input device for processing and after processing, it has to store (write) the data to memory or output device. Hence the data bus is bi-directional.	1	1	2
d.	Define instruction cycle, machine cycle and T state in microprocessor 8085. Answer : **Instruction Cycle:** The time required to execute an instruction is called instruction cycle. **Machine Cycle:** The time required to complete one operation of accessing the memory or input/output devices or acknowledging an internal request, is called machine cycle. **T-State:** A portion of an operation carried out in one system clock period is called as T-state.	1	2	1
e.	Draw flag register format of 8085 microprocessor. Answer : 	1	2	1

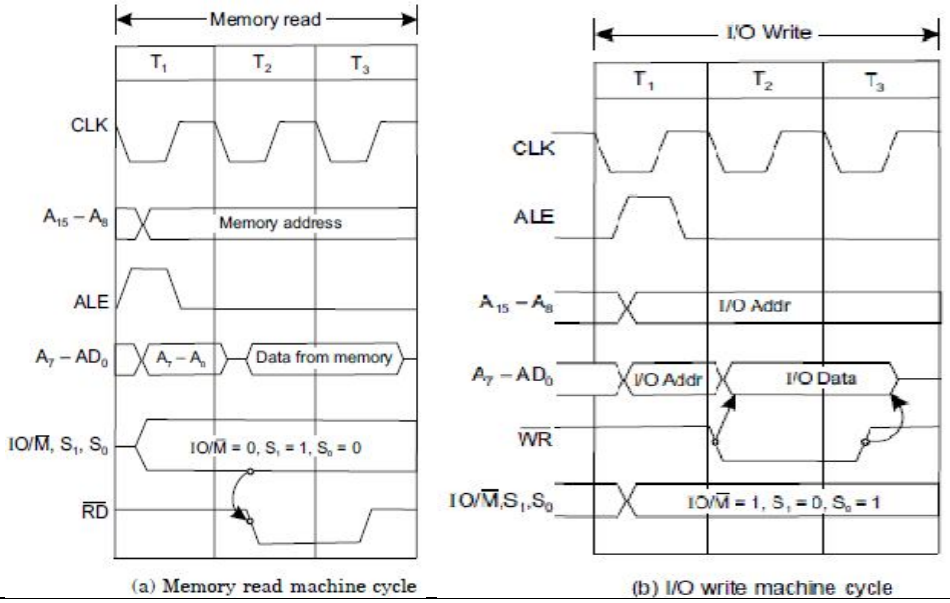
SECTION - B

2. Attempt any TWO of the following. **(2*5 = 10)**

Q N	QUESTION	Marks	CO	BL
a.	Describe evolution of microprocessor with its different generation. Answer : • The first Microprocessor (4004) was designed by Intel Corporation which was founded by Moore and Noyce in 1968. • With developments in integration technology Intel was able to integrate the additional chips like 8224 clock generator and the 8228 system controller along with 8080 microprocessor with in a single chip and released **the 8 bit microprocessor 8085 in the year 1976**. The 8085 microprocessor consisted of 6500 MOS transistors and could work at clock frequencies of 3-5 MHz. It works on a single +5 volts supply. • **In 1978, Intel introduced the 16 bit microprocessor 8086 and 8088 in 1979**. 8086 microprocessor made up of 29,000 MOS transistors and could work at a clock speed of 5-10 MHz. It has a 16-bit ALU with 16-bit data bus and 20-bit address bus. It can address up to 1MB of address space. The pipelining concept was used for the first time to improve the speed of the processor.	5	1	2

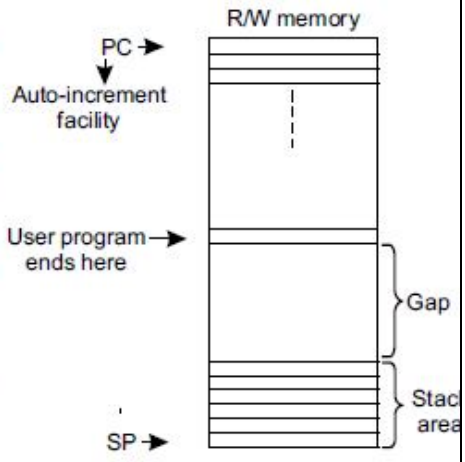
- **In 1982 Intel released another 16-bit processor called 80186 designed** by a team under the leadership of Dave Stamm. This is having higher reliability and faster operational speed but at a lower cost. It had a pre-fetch queue of 6-instructions and it is suitable for high volume applications such as computer workstations, word-processor and personal computers. It is made up of 134,000 MOS transistors and could work at clock rates of 4 and 6 MHz. This is also comes under first generation of Microprocessors.
- **Intel released another 16 bit microprocessor 80286 having** 1, 34,000 transistors in 1981. It was used as CPU in **PC-ATs in 1982**. It is the second generation microprocessor. It could run at clock speeds of 6 to 12.5 MHz .It has a 16-bit data bus and 24-bit address bus, so that it can address up to 16MB of address space and 1GB of virtual memory. It had a pre-fetch queue of 6 instructions .Intel introduced the concept of protected mode and virtual mode to ensure proper operation.
- **In 1985, Intel released the first 32 bit processor 80386**, with 275,000 transistors. It has 32-bit data bus and 32-bit address bus so that it can address up to a total of 4GB memory also a virtual memory space of 64TB.
- **Intel introduced 80486 microprocessor** with a built-in maths co-processor and with 1.2 million transistors. It could run at the clock speed of 50 MHz This is also a 32 bit processor but it is twice as fast as 80386.
- **On 19th October, 1992, Intel released the Pentium-I Processor** with 3.1 million transistors. So, the Pentium began as fifth generation of the Intel x86 architecture, the CPU is able to execute two instruction at the same time. The Pentium uses a 32-bit expansion bus, however the data bus is 64 bits.
- The 7.5 million transistors based chip, **Intel Pentium II processor was released in 1997**. It works at a clock speed of 300M.Hz. Pentium II uses the Dynamic Execution Technology which consists of three different facilities namely, Multiple branch prediction, Data flow analysis, and Speculative execution unit.
- **Intel Celeron Processors were introduced in the year 1999. Pentium-III** processor with 9.5 million transistors was introduced in 1999.
- **Pentium-IV with 42 million transistors and 1.5 GHz clock speed was released by Intel in November 2000.** The Pentium 4 processor has a system bus with 3.2 G-bytes per second of bandwidth.
- Intel with partner Hewlett-Packard developed the next generation **64-bit processor architecture called IA-64 .**This first implementation was named Itanium. Itanium processor which is the first in a family of 64 bit products was introduced in the year 2001.
- The **Itanium II is an IA-64 microprocessor** developed jointly by Hewlett-Packard (HP) and Intel and released on July 8,2002..It is theoretically capable of performing nearly 8 times more work per clock cycle than other CISC and RISC architectures due to its parallel computing micro-architecture.
- **Pentium 4EE** was released by Intel in the year 2003 and Pentium 4E was released in the year 2004.
- The **Pentium Dual Core**, which consists of 167 million transistors was released on January 21, 2007. Intel Core Duo consists of two cores on one die, a 2 MB L2 cache shared by both cores, and an arbiter bus that controls both L2 cache and FSB access.
- **In September.2009, new Core i7 models** based on the Lynnfield desktop quad-core processor and the Clarksfield quad-core mobile were added, and models based on the Arrandale dualcore mobile processor have been announced. The first six-core processor in the Core lineup is the Gulftown, which was launched on March 16, 2010.

b.	Draw the neat diagram of 8085 microprocessor architecture. ANSWER : The architecture of 8085 is shown below:  	**5**	**2**	**1**
c.	With neat diagram, explain the demultiplexing of lower-order address bus and data bus of 8085. ANSWER : • In 8085, lower-order address bus is time multiplexed with data bus. Pins AD7-AD0 act as lower-order address bus during T1 of opcode fetch machine cycle. After T1, these lines act as data lines, hence address is lost. To hold this address it is required to demultiplex lower-order address bus from data bus. • Following figure shows a schematic that uses a latch and ALE signal for demultiplexing. • Latch is enabled when ALE goes high, and address present at input lines is latched internally in respective D flip-flops.  	**5**	**2**	**2**

d.	Compare the memory read cycle and I/O write cycle of 8085 ANSWER :  (a) Memory read machine cycle (b) I/O write machine cycle	**5**	**2**	**3**

SECTION - C

3. Attempt any ONE part of the following : (1*5 = 5)

Q N	QUESTION	Marks	CO	BL
a.	Explain the function of control and status signals of 8085. Answer The control and status signals of 8085 are ALE, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$, S_0, S_1 i) The ALE (Address Latch Enable) is a signal used to demultiplex the address and data lines, using an external latch. It is used to enable the external latch. ii) IO/$\overline{M}$ signal indicates whether I/O or memory operation is being carried out. A high on this signal indicates I/O operation while a low indicates memory operation. iii) S_0 and S_1 indicate the type of machine cycle in progress. iv) $\overline{RD}$ (active low output) : The Read signal indicates that data are being read from the selected I/O or memory device and that they are available on the data bus. v) $\overline{WR}$ (active low output) : The Write signal indicates that data on the data bus are to be written into a selected memory or I/O location.	**5**	**2**	**2**
b.	Discuss the two registers program counter and stack pointer. Answer **Program counter (PC)** is a sixteen bit register which contains the address of the instruction to be executed just next. Program counter (PC) acts as a address pointer (also known as memory pointer) to the next instruction. As the processor executes instructions one after another, the PC is incremented—the number by which the PC increments depends on the nature of R/W memory the instruction. For example, for a 1-byte instruction, PC is incremented by one, while for a 3-byte instruction, the processor increments PC by three address locations. **Stack pointer (SP)** is a sixteen bit register which points to the 'stack'. The stack is an area in the R/W memory where temporary data or return addresses (in cases of subroutine CALL) are stored. The stack top is initialised by the SP by using the instruction LXI SP, memory address.  	**5**	**2**	**2**

S1	S0	States
0	0	Halt
0	1	Write
1	0	Read
1	1	Fetch

4. Attempt any ONE part of the following : **(1*5 = 5)**

Q N	QUESTION	Marks	CO	BL
a.	Compile the register content and the flag status after the instruction ORA A is executed. ANSWER MVI A, A9H — A = A9H MVI B, 57 H — B = 57 H ADD B — A = 00H ORA A — A = A9 H Flag Satus : CY =1, S = 1, and Z = 0	**5**	**2**	**3**
b.	Write an ALP to place the content of memory location A3ECH in register B and that of A3EDH in register C. The content of memory location A3ECH and A3EDH are EE H and EC H respectively. ANSWER : LXI H, A3EC — Get the content of memory address A3EC H in H-L pair MOV B,M — Move the content of A3EC H in register B INX H — Increament H – L pair by one. MOV C,M — Move the content of A3ED H in register C HLT — Halt Result : Content of Register B is EE H and Content of Register C is EC H	**5**	**2**	**3**

5. Attempt any ONE part of the following : **(1*5 = 5)**

Q N	QUESTION	Marks	CO	BL
a.	What do you mean by Addressing mode, explain different addressing mode used in 8085 with suitable example ANSWER : Each instruction indicates an operation to be performed on certain data. There are various methods to specify the data for the instructions, known as 'addressing modes'. For 8085 microprocessor, there are five addressing modes. These are: ***1. Direct Addressing:*** In this mode, the operand is specified within the instruction itself. ***Ex:*** LDA 4000 H, STA 5513H, etc. ***2. Register Addressing:*** The register addressing mode specifies the source operand, destination operand or both to be contained in an 8085 registers. ***Ex:*** MOV A,B ; ADD D, etc. **3. *Indirect Addressing:*** In this mode, the data in a register pair as a 16-bit address to identify the memory location being accessed. ***Ex:*** MOV A,M; ADD M, LDAX B etc. **4. *Immediate addressing mode:*** In this mode, 8 or 16 bit data can be specified as a part of instruction. ***Ex:*** MVI A,20H, LXI D,10FF H etc. **5. *Implied addressing mode:*** In implied addressing mode, Opcode specifies the address of the operands. ***Ex:*** CMA; RAL etc.	**5**	**2**	**2**
b.	Explain the following instructions of 8085 microprocessors i) PUSH PSW ii) XTHL iii) DAD B iv) MVI R, 8 bit v) CMP M ANSWER : Opcode Operand Byte M cycle T state i) PUSH Reg. pair 1 3 12 *Push register pair onto stack* ii) XTHL none 1 5 16 *Exchange H and L with top of stack* iii) DAD Reg. pair 1 3 10 *Add register pair to H and L registers* iv) MVI Reg. data 2 2 7 *Move immediate 8-bit* v) CMP M 1 2 7 Compare memory with accumulator	**5**	**2**	**2**