Dr. Kamal Prakash Pandey

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Professional Summary:

Qualification: M.Tech, P.h.D

Work Experience: 18years

Current Academic Designation: Associate Professor.

Organization: Shambhunath Institute of Engg. &Tech. Allahabad
(Affiliated to UPTU, Lucknow) Approved by AICTE, New Delhi

Specialization: VLSI DESIGN

Work Experience

- **Present Designation:** Teaching as a **"Associate Professor"** in the department of the Electronics & Communication Engg., "Shambhunath Institute of Engg. & Tech. Allahabad" from 2006 to till date.
- **Previous Designation**: Guest Lecturer from Aug 2001 – May, 2006-M. M. M. Engineering College Gorakhpur.

Teaching Proficiency

- Digital Electronics
- Electronics Engg.
- Integrated circuits
- VLSI Technology and design
- Digital system using VHDL

Job Profile:

- Currently acting as Dean PG at SIET Allahabad.
- Acting as Co-coordinator of M.Tech (VLSI design) in SIET Allahabad.
- Taking decision related to all administrative & student's related activities.
- Supervising the students in preparing dissertation, research papers & summer training reports.
- Providing personal counseling to the students related to their overall development and suggesting ways for their continuous improvement in the subject areas.

Educational Qualification:

- Ph.D from SHIATS, Allahabad in the field of VLSI Design.
- M.Tech in Instrumentation from N.I.T. Kurukshetra (Formerly REC Kurukshetra) Kurukshetra University in 2001,"**Title of the Thesis: "Design of PCI BUS Based DRAM Controller card in VHDL Environment"**
- B.E. (Electronics & Communication Engg**.)** From M.M.M.E.C Gorakhpur in 1999 from Gorakhpur University.

Publication/ Reviewer

- **Kamal Prakash Pandey**, Chandra Bhan, "Integrated Circuits" Published by Dhanpat Rai & CO. (P) LTD. ISBN 978-81-7700-037-5.
- **Kamal Prakash Pandey**, Chandra Bhan, Kulbhushan Gupta, "Electronics Engineering" Published by Dhanpat Rai & CO. (P) LTD. ISBN 978-81-7700-069-6.
- Review Questionnaire of VLSI Design offered by McGraw Hill education (VLSI Design by Partha Pratim Sahu) McGraw Hill Education (India) Private Limited.
- Working as active member of Editorial Board in the International Journal of Emerging Technology and Advanced Engineering.
- Working as active member of Review Board in the International Journal of Research in Engineering and Technology.

Publications in International Journals

1. Mayank Kumar, Mukesh Kumar, Anil Kumar, Ashish Das, A. K. Jaiswal, Gaurav Nigam, **Kamal Prakash Pandey**, "An Improved Device Consideration for Ultra-Low Power Applications in Junction Field Effect Transistor." International Journal of Emerging Technology and Advanced Engineering, Volume 3, Issue 2, February 2013 (ISSN 2250-2459), pp No.292-295.
2. Gaurav Nigam, Anil Kumar, Mukesh Kumar, A. K. Jaiswal, Mayank Kumar, **Kamal Prakash Pandey**, Atishay Dixit**,** "Analytical Model for Thin Depleted SOI Enhancement MOSFET**.**" International Journal of Emerging Technology and Advanced Engineering, Volume 3, Issue 2, February 2013 (ISSN 2250-2459), pp No.245-249.
3. Imran Yusuf, Rajeev Paulus, Mayur Kumar, A. K. Jaiswal, Anil Kumar, **Kamal Prakash Pandey,** "Analytical Study of Impedance Matching for Probe Fed Rectangular Microstrip Patch Antenna." International Journal of Engineering and Innovative Technology, Volume 2, Issue 10, April 2013, (ISSN 2277- 3754), pp No.51-53.
4. **Kamal Prakash Pandey**, Rakesh Kumar Singh, Anil Kumar, "Analyzed Modulation Doped Field Effect Transistor (MODFET) and Metal Oxide Semiconductor Modulation Doped Field Effect Transistor (MOS-MODFET) using compound material silicon Germanium (SiGe)".

International Journals of Advanced Research in Computer and Communication Engineering. Volume 2, Issue 4, April 2013 (ISSN 2278-1021), pp No.1831-1834.

5. **Kamal Prakash Pandey**, Rakesh Kumar Singh, Anil Kumar**,** "Analytical Study of Radial Gap Capacitance for Probe Feed Rectangular Microstrip Patch Antenna." International Journal of Innovative Research in Computer and Communication Engineering. Volume 1, Issue 2, April 2013, (ISSN 2320-9801) pp No.170-174.
6. Rakesh Kumar Singh, **Kamal Prakash Pandey**, Abhishek Kumar Pandey, Chandrabhan, Anil Kumar**,** "Analytical Study of Capacitance Extraction of MOSFET". International Journals of Advanced Research in Computer and Communication Engineering. Volume 2, Issue 7, July 2013 (ISSN 2278-1021), pp No.2855-2858.
7. **Kamal Prakash Pandey,** Rakesh Kumar Singh, Surendra Kumar Tadi, Anil Kumar, "A Novel approach of identifying uninitialized register in SOC Designs." International Journals of Advanced Research in Computer and Communication Engineering. Volume 2, Issue 8, August 2013 (ISSN 2278-1021), pp No.3193-3196.
8. **Kamal Prakash Pandey**, Rakesh Kumar Singh, Surendra Kumar Tadi, "Clock Domain Crossing Verification in a System on Chip." "International Journal of Emerging Technology and Advanced Engineering." Volume 4, Issue 1, January 2014, (ISSN 2250- 2459), pp No.617-622.
9. Sandeep Kumar Ojha, **Kamal Prakash Pandey**, Rakesh Kumar Singh, "Design, Test and Testability on VLSI Circuits" "International Journal of Emerging Technology and Advanced Engineering." Volume 4, Issue 8, August 2014, (ISSN 2250- 2459), pp No.689-691.
10. Kamlesh Kumar Dwivedi, **Kamal Prakash Pandey**, Rakesh Kumar Singh, Kulbhusan Gupta, "Design and Analysis of CMOS Multiplier and EEAL Multiplier for Low Power VLSI Application. "International Journal of Emerging Technology and Advanced Engineering." Volume 4, Issue 9, September 2014, (ISSN 2250- 2459), pp No.424-428.
11. **Kamal Prakash Pandey**, Vishal Yadav, "Design and Analysis of Latch Sense Amplifier". International Journal of Emerging Technology and Advanced Engineering." Volume 4, Issue 12, December 2014, (ISSN 2250- 2459), pp No.508-512.
12. Shikha Shukla, **Kamal Prakash Pandey**, Rakesh Kumar Singh, "Implementation and Simulation of Low Pass Finite Impulse Response Filter Using Different Window Method." International Journal of Emerging Technology and Advanced Engineering." Volume 5, Issue 1, January 2015, ISSN 2250- 2459, pp No.88-93.
13. **Kamal Prakash Pandey**, Kamlesh Kumar Dwivedi, Kamlesh Kumar Yadav, "Design and Comparative Analysis of EEAL Sequential Circuit for Low Power VLSI Application. "International Journal of Emerging Technology and Advanced Engineering." Volume 5, Issue 3, March 2015, ISSN 2250- 2459, pp No.317-321.
14. Rajesh Kumar Dubey, **Kamal Prakash Pandey**, Rakesh Kumar Singh, "CIC Decimation Filter for Frequency. "International Journal of Science and Research (IJSR)." Volume 4 Issue 9, September 2015, ISSN 2319-7064. pp No. 1401-1405.
15. Aditya Kumar Singh, **Kamal Prakash Pandey**, Vivek Singh, "Representation and Conversion of Line Coding using Mealy Sequential Network. " International Journal of emerging trends in Engineering and Development (IJETED). Issue 6, Vol. 1 January 2016, ISSN 2249-6149. pp No. 76-81.

16. Mona Sachan, **Kamal Prakash Pandey**, Rakesh Kumar Singh, "Design and Analysis of Fin Field Effect Transistor with Complex Semiconductor Material as SiGe." International Journal of Emerging Technology and Advanced Engineering. Volume 6, Issue 2, February 2016. ISSN 2250-2459, pp No. 146-150.

17. **Kamal Prakash Pandey,** Rakesh Kumar Singh, "High Performance Hardware Realization of Advanced Encryption Standard." International Journal of Science and Research (IJSR), Volume 5 Issue 4, April 2016, ISSN 2319-7064, pp No- 428-431.

18. Jitendra Kumar, Devendra Kumar Tripathi, **Kamal Prakash Pandey,** "Performance Analysis of Optical IDMA by using Different type of photodectors." International Journal of Emerging Technology and Advanced Engineering, Volume 6, Issue 3, March 2016, ISSN 2250- 2459, pp No. 282-286.

19. **Kamal Prakash Pandey,** Sandip Ranjan Sahaya, "Comparative Study of PMOS Field Effect Transistor and Silicon on Insulator PMOS Field Effect Transistor." International Journal of Emerging Technology and Advanced Engineering, Volume 6, Issue 9, September 2016, ISSN 2250- 2459, pp No. 89-91.

20. Anush Bekal, Saloni Varshney, **Kamal Prakash Pandey** and Manish Goswami "Linear Relationship ADC with Complimentary Switch Based Bootstrapped Sample and Hold Circuit," International Journal of Electronics (**SCI Indexed)**), Volume104, Issue9, pp.1227-1246, 2017.

21. **Kamal Prakash Pandey,** Anil Kumar, "Design and Analysis of dual Axis MEMS Capacitive Accelerometer", International Journal of Electronics Engineering Research (**Scopus Indexed**) Volume 9, Number 5 pp. 779-790, 2017.

22. Devendra Kumar Tripathi, **Kamal Prakash Pandey,** "Investigations with All Optical NOT Logic Gate", International Journal of Emerging Technology and Advanced Engineering, Volume 7, Issue 6, pp.126-131, June 2017.

23. Devendra Kumar Tripathi, **Kamal Prakash Pandey,** "Design and Study with Optical XOR/XNOR Network", International Journal of Emerging Technology and Advanced Engineering, Volume 7, Issue 6, pp.132-136, June 2017.

24. **Kamal Prakash Pandey** , Anil Kumar , A.K. Jaiswal, "Design and Simulation of Nano Scale FIN FET using Silvaco TCAD", International Journal of Emerging Technology and Advanced Engineering, Volume 7, Issue 6, pp.275-282, June 2017.

25. **Kamal Prakash Pandey** , Anil Kumar , A.K. Jaiswal, "Design and Simulation of High Electron Mobility Transistor using Silvaco TCAD", International Journal of Emerging Technology and Advanced Engineering, Volume 7, Issue 6, pp.283-287, June 2017.

26. Chahat Varshney, **Kamal Prakash Pandey**, Naresh Chandra Agrawal, "Design and Implementation of Smart Vending Machine with security Features for Automatic car Parking System", International Journal of Advanced Engineering Research and Technology (IJAERT) Volume 5 Issue 8, pp.643-647 August 2017.

27. Mehreen, **Kamal Prakash Pandey**, "Design and Implementation of Low Leakage - Power-Optimized Reversible Arithmetic Circuits Using PERES & DOMINO", International Journal of Advanced Engineering Research and Technology (IJAERT) Volume 5 Issue 8, pp.648-651, August 2017.

28. Nasreen, **Kamal Prakash Pandey**, D. K. Tripathi, "Design of 32-bit Reversible Booth Multiplier and Area Optimization using Genetic Algorithm", International Journal of Emerging Technology and Advanced Engineering, Volume 7, Issue 8, pp.423-426, August 2017.

29. Kumudlata Bhaskar, **Kamal Prakash Pandey,** Chandrabhan, "A VLSI Implementation For High Speed And High Sensitive Fingerprint Sensor Using Charge Acquisition Principle", International Journal Of Engineering Sciences & Research Technology, Volume 6, Issue 9, pp.555-560, September 2017.

30. Virendra Kumar Yadav, **Kamal Prakash Pandey**, Vikrant Varshney, "Zero Temperature-Coefficient Bias Point for Asymmetrical and Symmetrical Double Metal Double Gate MOSFETs", International Journal for Research in Applied Science & Engineering Technology (IJRASET), Volume 5 Issue 12, pp.1140-1147, December 2017.

31. **Kamal Prakash Pandey**, Gunjan Agrawal, "Design And Implementation of High Speed Scan-Hold Flip Flop based Shift Registers", International Journal of Advance Engineering and Research Development, Volume 4, Issue 12, pp.640-647, December -2017.

32. **Kamal Prakash Pandey**, Apoorv Upadhyay, "Design And Implementation of SPI Protocol," International Journal of Advance Engineering and Research Development, Volume 4, Issue 12, pp.1010-1016, December -2017.

33. **Kamal Prakash Pandey**, Harshit Swaroop, Chandrabhan, "Performance Analysis of Vedic Multiplier Based on Various Adders" International Journal of Engineering Research in Computer Science and Engineering (IJERCSE), Vol 5, Issue 1, January 2018, pp 42 – 46.

34. **Kamal Prakash Pandey**, Pradumn Kumar, Rakesh Kumar Singh, "Performance Enhancement of Reversible Binary to Gray Code Converter Circuit using Feynman gate", International Journal for Research in Applied Science & Engineering Technology (IJRASET), Volume 6 Issue I, January 2018, pp. 1775 – 1783.

35. Upendra Kashniyal**, Kamal Prakash Pandey,** "Stress induced degradation and reliability of Al_2O_3 thin film on silicon" Elsevier Vacuum (**SCI Indexed**), Vacuum 152 (2018) pp. 109-113.

36. **Kamal Prakash Pandey,** "Memory improvement in lead-free BiFeO3 ferroelectric with high-k Al2O3 buffer layer for non-volatile memory applications" Applied Physics A Springer(**SCI Indexed)** Volume 124, Issue 7, July 2018 pp.1-8

37. **Kamal Prakash Pandey,** "Device Simulation of Si-Ge HBT Using SILVACO TCAD", International Journal of Computer Sciences and Engineering, Vol.-6, Issue-5, May 2018,pp. 331-335

Conference/Workshop/FDP

- Actively Participated in workshop on "Essential of plan Ahead"Organised by Indian Institute of Technology, Delhi Dated on 10/12/2011
- Actively Participated in workshop on "Application of Qualnet in wireless network" Organised by SHIATS-DU, Allahabad, U.P. Dated on 23-24 Aug-2012
- Actively Participated in workshop on "Advance VLSI Design Automation" Organised by SHIATS-DU, Allahabad, U.P. Dated on 08/09/2012
- Actively Participated in International workshop on "Antenna & RF Design for Low Power Applications"Organised by IIIT Allahabad, U.P. Dated on September 27-30, 2012.

- Actively Participated in Two Weeks Faculty Development Programme on "Simulation and Mathematical Tools for Engineering Research", Organized by K.N.I.T. Sultanpur, U.P., Dated on 04 July to 15 July 2016 sponsored by AICTE.
- Actively Participated in One Week Faculty Development Programme on "Recent Advances in Renewable Energy Technologies & Smart Micro-grids", Under TEQIP-II. Organized by K.N.I.T. Sultanpur, U.P., Dated on 13 September to 17 September2016.
- Actively Participated in One Week International workshop on "Antenna Design and Signal Processing Techniques for 5G Networks and IoT" Organized by MNNIT Allahabad and IEEE MNNIT Student Branch, Dated on February 27 to 4 March, 2017.
- Actively Participated in One Week International workshop on "Communication and Antenna Design for IoT" Organized by MNNIT Allahabad and IEEE MNNIT Student Branch, Dated on 22-27 September, 2017.
- Paper entitled **"**Design and Analysis of MEMS Varactor" presented in IEEE International conference on recent advances in engineering, technology and computational sciences 2018(RATECS 2018).
- Upendra Kashniyal, Kamal Prakash Pandey, Rakesh Kumar Singh"Stress Induced Degradation and Reliability of Ta2O5 thin film on Silicon", 19thInternational Workshop on the Physics of Semiconductor Devices, IITDelhi, India, Dec. 2017sponsored by Springer.

Administrative / Academic Post Held at University Level

1. Worked as Centre Controller in SEE-2007-10 and UPSEE- 2014, UPTU.
2. Worked as Nodal Officer in UPSEE-2014.
3. Worked as Deputy Head Examiner in GBTU evaluations in 2011 and 2012.
4. Worked as Group Leader for M.Tech/M.Pharma examination in UPTU-2015.
5. Worked as Paper Setter in Electronics & Communication Engineering Subjects of various Universities i.e. M J P Rohilkhand University, Bareilly, Poorvanchal University, Jaunpur, SHIATS, Allahabad.
6. Worked as evaluator in Electronics & Communication Engineering Subjects of various Universities i.e. M J P Rohilkhand University, Bareilly, Poorvanchal University, Jaunpur, SHIATS, Allahabad.

M.Tech. Supervised

12 Completed
02Under Progress

Membership of Professional Societies:

1. Member of IEEE
2. Life Member of ISTE

Extra Curricular Activity

- Active member of N.S.S.
- Captain of college cricket team, won inter engineering college cricket tournament in 1999.

Personal Details:

Father's name	:	Shri R. D. Pandey
Date of birth	:	3 June 1974
Mailing Address	:	SIET, JHALWA CAMPUS, Distt. Allahabad–211012, (U.P.), India
Nationality	:	Indian

References:

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Professor
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Department of Electronics and Communication Engineering IET Lucknow,
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Mob. No. +919451215400.

I hereby declare that the above information given is true and correct to the best of my knowledge.

DATE : 19 July 2018

PLACE: Allahabad **Dr. Kamal Prakash Pandey**